

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

Japanese Patent Laid-Open Publication No. Heisei 9-8205

(TITLE OF THE INVENTION)

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

5

(CLAIMS)

1. A resin-encapsulated semiconductor device using  
a lead frame which is shaped in accordance with a two-step  
etching process to a body wherein a thickness of inner  
10 leads is less than that of the lead frame blank,  
comprising:

inner leads having the thickness less than that of the  
lead frame blank; and

15 terminal columns integrally connected to the inner  
leads and having the same thickness with the lead frame  
blank, the terminal columns possessing a column-shaped  
configuration which is adapted to be electrically connected  
to an external circuit, the terminal columns being disposed  
outside of the inner leads in a manner such that they are  
20 coupled to the inner leads in a direction orthogonal to the  
thickness-wise direction thereof, the terminal columns  
having terminal portions arranged on top ends thereof, the  
terminal portions being made of solders, etc. and exposed  
to the outside beyond a resin encapsulate, each inner lead  
25 possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a  
third surface and a fourth surface, the first surface being  
flushed with one surface of a remaining portion of the  
inner lead having the same thickness with the lead frame  
blank while being opposed to the second surface, and each  
5 of the third and fourth surfaces having a concave shape  
depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using  
10 a lead frame which is shaped in accordance with a two-step  
etching process to a body wherein a thickness of inner  
leads is less than that of the lead frame blank,  
comprising:

inner leads having the thickness less than that of the  
15 lead frame blank; and

terminal columns integrally connected to the inner  
leads and having the same thickness with the lead frame  
blank, the terminal columns possessing a column-shaped  
configuration which is adapted to be electrically connected  
20 to an external circuit, the terminal columns being disposed  
outside of the inner leads in a manner such that they are  
coupled to the inner leads in a direction orthogonal to the  
thickness-wise direction thereof, portions of top ends of  
the terminal columns being exposed to the outside beyond a  
25 resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank, while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

10 3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

15 4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

20 5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

25 6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513  
to be electrically connected to the associated circuits,  
inner leads 1512 formed integrally with the outer leads  
1513, bonding wires 1530 for electrically connecting the  
5 tips of the inner leads 1512 to the bonding pad 1521 of the  
semiconductor chip 1520, and a resin 1540 encapsulating the  
semiconductor chip 1520 to protect the semiconductor chip  
1520 from external stresses and contaminants. This resin-  
encapsulated semiconductor device, after mounting the  
10 semiconductor chip 1520 on the bonding pad 1521, is  
manufactured by encapsulating the semiconductor chip 1520  
with the resin. In this resin-encapsulated semiconductor  
device, the number of the inner leads 1512 is equal to that  
of the bonding pads 1521 of the semiconductor chip 1520.  
15 And, FIG. 15(b) shows the configuration of a monolayer lead  
frame used as an assembly member of the resin-encapsulated  
semiconductor device shown in FIG. 15a. Such a lead frame  
includes the bonding pad 1511 for mounting the  
semiconductor chip, the inner leads 1512 to be electrically  
20 connected to the semiconductor chip, the outer lead 1513  
which is integral with the inner leads 1512 and is to be  
electrically connected to the associated circuits. This  
also includes dam bars 1514 serving as a dam when  
encapsulating the semiconductor chip with the resin, and a  
25 frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

10 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).



Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80  $\mu$ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged pitches in the range of 0.13 to 0.15 mm, far smaller to 0.165 mm. When a lead frame is fabricated by processing thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half etching or pressing to form the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

15 (SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

5 According to one aspect of the present invention, there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular cross-section and having four surfaces including a

10

15

20

25

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surf-  
of a remaining portion of the inner lead having the same  
thickness with the lead frame blank while being opposed  
5 the second surface, and each of the third and fourth  
surfaces having a concave shape depressed toward the first  
of the inner lead.

According to another aspect of the present invention  
there is provided a resin-encapsulated semiconductor device  
10 using a lead frame which is shaped in accordance with  
two-step etching process to a body wherein a thickness  
inner leads is less than that of the lead frame blank  
comprising: inner leads having the thickness less than that  
of the lead frame blank; and terminal columns integrally  
15 connected to the inner leads and having the same thickness  
with the lead frame blank, the terminal columns possessing  
a column-shaped configuration which is adapted to be  
electrically connected to an external circuit, the terminal  
columns being disposed outside of the inner leads in a  
20 manner such that they are coupled to the inner leads in a  
direction orthogonal to the thickness-wise direction  
thereof, portions of top ends of the terminal columns being  
exposed to the outside beyond a resin encapsulate, outer  
surfaces of the terminal columns also being exposed to the  
25 outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

#### 20 [WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

#### [EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance



with a first embodiment of the present invention  
described hereinafter with reference to FIGS. 1  
FIG. 1(a) is a cross-sectional view of the  
encapsulated semiconductor device according to the  
embodiment of the present invention. FIG. 1(b) is a  
sectional view of an inner lead taken along the line  
of FIG. 1(a), and FIG. 1(c) is a cross-sectional view  
terminal column taken along the line B1-B2 of FIG.  
Moreover, FIG. 2(a) is a perspective view of the  
encapsulated semiconductor device according to the  
embodiment of the present invention, FIG. 2(b) is a  
view of the resin-encapsulated semiconductor device of  
2(a), and FIG. 2(c) is a bottom view of the  
encapsulated semiconductor device of FIG. 2(a). In F  
and 2, a drawing reference numeral 100 represents a  
encapsulated semiconductor device, 110 a semicond  
chip, 111 electrodes (pads), 120 wires, 130 a lead  
131 inner leads, 131Aa a first surface, 131Ab a s  
surface, 131Ac a third surface, 131Ad a fourth surface  
terminal columns, 133A terminal portions, 133B  
surfaces, 133S a top surface, 135 a die pad, and  
resin encapsulate.

In the resin-encapsulated semiconductor de  
according to the first embodiment, as shown in FIG. 1  
the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 133 at one surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131a of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133a each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133a located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9 is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40  $\mu$ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the  
inner leads 131 is long or not. The inner leads having the  
contour, as shown in FIG. 9(a), in which the tips of the  
inner leads 131 are separated one from another, are  
5 prepared by the etching process, and the inner leads are  
resin-encapsulated after mounting the semiconductor chip  
thereon as will be described later. However, where the  
inner leads 131 are long in their length and have a  
tendency for the generation of twisting therein, it is  
10 impossible to fabricate the lead frame by etching to have  
the contour as shown in FIG. 9(a). Therefore, after  
etching the lead frame in a state where the tips of the  
inner leads are fixed to the connecting portion 131B as  
shown in FIG. 9(c)(1), the inner leads 131 are fixed with  
15 the reinforcing tape 160 as shown in FIG. 9(c)(2). Then,  
the connecting portions 131B which are not necessary in the  
fabrication of the resin-encapsulated semiconductor device  
are removed by a press as shown in FIG. 9(c)(3), and a  
semiconductor device is then mounted on the lead frame.

20 Hereinafter, a method for the fabrication of the  
resin-encapsulated semiconductor device will now be  
described with reference to FIG. 8. First, the lead frame  
130A, as shown in FIG. 9(a), which is shaped by the etching  
process as will be described later, is prepared such that  
25 the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131Ab of the inner leads 131 are bonded with each other using wires 120 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby (FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However, persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160  
second concave portions, 1170 flat surfaces, and 1180 an  
etch-resistant layer. First, a water-soluble casein resist  
using potassium dichromate as a sensitive agent is coated  
5 over both surfaces of the lead frame blank 1110 made of a  
42% nickel-iron alloy and having a thickness of about 0.15  
mm. Using desired pattern plates, the resist films are  
patterned to form resist patterns 1120A and 1120B having  
first opening 1130 and second openings 1140, respectively  
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead  
frame blank 1110 to have a flat etched bottom surface to a  
thickness smaller than that of the lead frame blank 1110 in  
a subsequent process. The second openings 1140 are adapted  
15 to form desired shapes of tips of inner leads. Although  
the first opening 1130 includes at least an area forming  
the tips of the inner leads 1110, a topology generated by  
partially thinned portion by etching in a subsequent  
process can cause hindrance in a taping process or a  
20 clamping process for fixing the lead frame. Thus, an area  
to be etched needs to be large without being limited to  
fine portions of the tips of the inner leads. Thereafter,  
both surfaces of the lead frame blank 1110 formed with the  
resist patterns are etched using a 48 Be' ferric chloride  
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm<sup>2</sup>. The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth  $h$  corresponding to  $1/3$  of the thickness of the lead frame blank (FIG. 11a).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in  
10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the  
15 resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant  
20 layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that  
25 the etch-resistant layer 1180 be coated over the entire



portion of the surface formed with the first recesses  
and first opening 1130, as shown in FIG. 11(c), because  
it is difficult to coat the etch-resistant layer 1180 on  
the surface portion including the first recesses.  
5 Although the etch-resistant layer 1180 wax employed in  
this embodiment is an alkali-soluble wax, any material  
resistant to the etching action of the etchant solution  
remaining somewhat soft during etching may be used.  
for forming the etch-resistant layer 1180 is not limited  
10 to the above-mentioned wax, but may be a wax of a UV-se  
type. Since each first recess 1130 etched by the pre-  
etching process at the surface formed with the paste  
is adapted to form a desired shape of the inner lead track,  
filled up with the etch-resistant layer 1180, it is  
15 further etched in the following secondary etching process.  
The etch-resistant layer 1180 also enhances the mechanical  
strength of the lead frame blank for the second etching  
process, thereby enabling the second etching process to be  
conducted while keeping a high accuracy. It is  
20 possible to enable a second etchant solution to be sprayed  
at an increased spraying pressure, for example, 2.5 kg  
or above, in the secondary etching process. The increased  
spraying pressure promotes the progress of etching in the  
direction of the thickness of the lead frame blank in  
25 secondary etching process. Then, the lead frame blank

portion of the surface formed with the first recesses  
and first opening 1130, as shown in FIG. 11(c), because  
it is difficult to coat the etch-resistant layer 1180 on  
the surface portion including the first recesses.  
5 Although the etch-resistant layer 1180 wax employed in  
this embodiment is an alkali-soluble wax, any suitable  
wax resistant to the etching action of the etchant solution  
remaining somewhat soft during etching may be used.  
The method for forming the etch-resistant layer 1180 is not limited  
10 to the above-mentioned wax, but may be a wax of a UV-sensitive  
type. Since each first recess 1150 etched by the primary  
etching process at the surface formed with the pattern is  
adapted to form a desired shape of the inner lead track,  
filled up with the etch-resistant layer 1180, it is  
15 further etched in the following secondary etching process.  
The etch-resistant layer 1180 also enhances the mechanical  
strength of the lead frame blank for the second etching  
process, thereby enabling the second etching process to be  
conducted while keeping a high accuracy. It is  
20 possible to enable a second etchant solution to be sprayed  
at an increased spraying pressure, for example, 2.5 kg/cm<sup>2</sup>  
or above, in the secondary etching process. The increased  
spraying pressure promotes the progress of etching in the  
direction of the thickness of the lead frame blank in the  
25 secondary etching process. Then, the lead frame blank

In this  
FIG. 11(c) is  
seen that the  
completely  
forming the  
  
defined by the  
on both sides  
of the  
directed toward  
the blank  
ess, the  
(resist  
Thus,  
FIG. 9(a) is  
arranged  
that layer  
120B) is  
viewing to  
  
same as  
the lead  
in this  
thickness  
the first

surfaces 131Aa of the tips of the inner leads as shown in  
FIG. 1, are flushed with one surfaces of remaining portions  
of the inner leads having the same thickness with the lead  
frame while being opposed to the second surfaces 131Ab, and  
the third and fourth surfaces are formed to have a concave  
shape which is depressed toward the inside of the inner  
leads. Where a semiconductor chip is mounted on the second  
surfaces 131Ab of the inner leads by means of bumps for an  
electrical connection therebetween, as in a semiconductor  
device according to a third embodiment as will be described  
hereinafter, an increased tolerance for the connection by  
bumps is obtained when the second surface 131Ab has a  
concave shape depressed toward the inside of the inner  
lead. To this end, an etching method shown in FIG. 12 is  
adopted in this case. The etching method shown in FIG. 12  
is the same as that of FIG. 11 in association with its  
primary etching process. After completion of the primary  
etching process, the etching method is conducted in a  
manner different from that of the etching method of FIG. 11  
in that the second etching process is conducted at the side  
of the first recesses 1150 after filling up the second  
recesses 1160 by the etch-resist layer 1180, thereby  
completely perforating the second recesses 1160. At this  
time, by implementing the primary etching process, etching  
at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Aa, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness  $t$  of the inner lead tip which is finally obtained. For example, where the blank has a thickness  $t$  reduced to 50  $\mu\text{m}$ , the inner leads can have a fineness corresponding to a lead width  $W_1$  of 100  $\mu\text{m}$  and a tip pitch  $p$  of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness  $t$  of about 30  $\mu\text{m}$  and a lead

width  $W_1$  of 70  $\mu\text{m}$ , it is possible to form inner leads having a fineness corresponding to an inner lead pitch  $p$  of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness  $t$  and the lead width  $W_1$ . That is to say, an inner lead tip pitch  $p$  up to 0.08 mm, a blank thickness up to 25  $\mu\text{m}$ , and a lead width  $W_1$  up to 40  $\mu\text{m}$  can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(c)(A)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W1 slightly greater than the width W2 of an opposite surface. The widths W1 and W2 (about 1000  $\mu$ m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(D)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(A) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(B) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(B). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(B)(a) or FIG. 13(B)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified



example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGs. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of  
this third embodiment, the semiconductor chip 310 is  
fastened to the second surfaces 331Ab of the inner leads  
331 by the bumps 311 thereby to be electrically connected  
5 to the second surfaces 331Ab. The lead frame 330 has a  
contour as shown in FIGs. 10(a) and 10(b), which is formed  
by the etching process of FIG. 11. As shown in FIG.  
13(1)(b), both widths W1A and W2A (about 100  $\mu$ m) at top  
and bottom ends of the inner leads 331 are larger than a  
10 width WA at a center portion in a thickness-wise direction.  
Due to the fact that the second surfaces 331Ab of the inner  
leads 331 is depressed toward the inside of the inner leads  
and the first surfaces 331Aa are flat, a desired fineness  
can be obtained. Also, when the second surfaces 331Ab of  
15 the inner leads 331 are electrically connected to the  
semiconductor chip via bumps, easy connection can be  
accomplished as shown in FIG. 13(D)(b). Further, in the  
case of this third embodiment, as in the case of the first  
and second embodiments, the electrical connection between  
20 the resin-encapsulated semiconductor device 300 of this  
embodiment and an external circuit is achieved by mounting  
the resin-encapsulated semiconductor device 300 via the  
terminal portions 333A each being made of a semi-spherical  
solder, on a printed circuit substrate, with the terminal  
25 portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line 10 B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing 15 reference numeral 400 represents a semiconductor device, 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth 20 embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second 25

surfaces 431Ab of the inner leads 431 by the insul-  
adhesive 470, and the pads 411 and the first surfaces  
of the inner leads 431 are electrically connected with  
other by wires 420. The semiconductor device of  
5 fourth embodiment uses the same lead frame which is use  
the third embodiment, which has the contour as shown  
FIG. 10(a) and 10(b). Also, in the case of this fourth  
embodiment, as in the case of the first and second  
embodiments, the electrical connection between the res-  
10 encapsulated semiconductor device 400 of this embodiment  
and an external circuit is achieved by mounting the res-  
encapsulated semiconductor device 400 via the terminal  
portions 433A each being made of a semi-spherical solder  
on a printed circuit substrate, with the terminal portion  
15 433A located on the top surfaces of the terminal columns  
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating  
modified example of the semiconductor device in accordance  
with the fourth embodiment of the present invention. In  
20 the modified example of the semiconductor device as shown  
in FIG. 7(d), the terminal portions each comprising the  
semi-spherical solder are not provided, and the top  
surfaces of the terminal columns are directly used as the  
terminal portions. Because the protective frame is not  
25 used and the side surfaces 433B of the terminal columns 433



are exposed to the outside, a checking operation by a test, etc. can be easily performed.

#### (EFFECTS OF THE INVENTION)

5       The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay time.

10  
15  
20

59:543 v:

59:543 v:

(11) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(13) 特許公開番号

特開平 9-8205

(14) 公報日 平成 9 年 (1997) 1 月 15 日

(51) Int. Cl.

H01L 13/50

出願番号

特願 95-170490

F I

H01L 13/50

特許庁長官

13/11

13/11

審査請求 異議 再審査の請求 F D 全 1 5 頁

(11) 出願番号 特願 95-170490

(12) 出願日 平成 7 年 (1995) 6 月 14 日

(13) 出願人 000002897

大日本印刷株式会社

東京都港区新橋 3-1-1 丁目 1 番 1 号

(14) 発明者 山田 成一

東京都港区新橋 3-1-1 丁目 1 番 1 号

大日本印刷株式会社内

(15) 発明者 佐々木 賢

東京都港区新橋 3-1-1 丁目 1 番 1 号

大日本印刷株式会社内

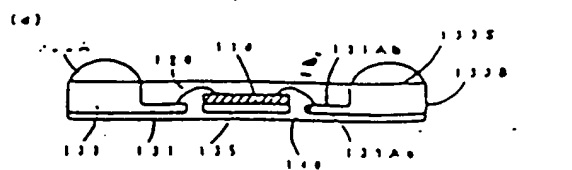
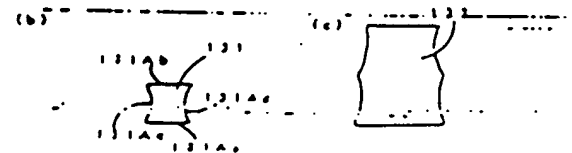
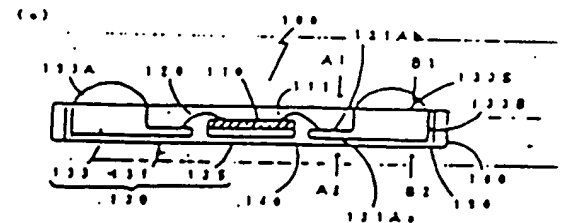
(16) 代理人 弁護士 小西 成典

(34) [発明の名称] 読取防止型半導体装置

(37) [要約] (形証書)

[目的] 多素子化に対応でき、且つ、アフターリードの位置ズレや半導体の向きにも対応できる読取防止型半導体装置を提供する。

[構成] 一体的に形成したリードフレーム部材と同じ厚さの外部回路と積層するための凸状の端子部 133 とを有し、且つ、端子部はインナーリードの外側にあり、インナーリードに対して厚み方向に突出して設けられており、端子部の先端面に半導体からなる素子部を設け、端子部を防止層部から突出させ、端子部の外部側の側面を防止層部から突出させており、インナーリードは、断面形状が略円形で第 1 図 131 A a、第 2 図 A b、第 3 図 A c、第 4 図 A d の 4 面を有しており、かつ第 1 図はリードフレーム部材と同じ厚さの絶縁部材の一方の面と同一平面上にあって第 2 図に面を有しており、第 3 図、第 4 図はインナーリードの内側に向かって凹んだ形状に形成されている。



## 【実施例の概略】

【図3例1】 2段ニッチング加工によりインターリードの厚さがリードフレーム素材の厚さより厚み状に形成されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム素材より厚み状のインターリードと、該インターリードに一時的に透過したリードフレーム素材と同じ厚さの外周部材とを形成するための仕様の導子柱とを有し、且つ、導子柱はインターリードの外周部材においてインターリードに対して厚み方向に偏装して設けられており、導子柱の先端部に半導体からなる導子部を設け、導子部を前記厚み状部材から露出させ、導子柱の外周部材の側面を前記厚み状部材から露出させており、インターリードは、表面形状が四方形で第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第2面に向を合っており、第3面、第4面はインターリードの内側に所かつて凹んだ形状に形成されていることを特徴とする厚み状半導体装置。

【図3例2】 2段ニッチング加工によりインターリードの厚さがリードフレーム素材の厚さより厚み状に形成されたリードフレームを用いた半導体装置であつて、前記リードフレームは、リードフレーム素材より厚み状のインターリードと、該インターリードに一時的に透過したリードフレーム素材と同じ厚さの外周部材とを形成するための仕様の導子柱とを有し、且つ、導子柱はインターリードの外周部材においてインターリードに対して厚み方向に偏装して設けられており、導子柱の先端の一部を前記厚み状部材から露出させて導子部とし、導子柱の外周部材の側面を前記厚み状部材から露出させており、インターリードは、表面形状が四方形で第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第2面に向を合っており、第3面、第4面はインターリードの内側に所かつて凹んだ形状に形成されていることを特徴とする厚み状半導体装置。

【図3例3】 図3例1ないし2において、半導体素子はインターリード間に設けられ、該半導体素子の電極部はワイヤにてインターリードと電気的に接続されていることを特徴とする厚み状半導体装置。

【図3例4】 図3例3において、リードフレームはダイパッドを有しており、半導体素子はダイパッド上に設けられ、固定されていることを特徴とする厚み状半導体装置。

【図3例5】 図3例3において、リードフレームはダイパッドを有しないもので、半導体素子はインターリードとともに基板固定用テープにより固定されていることを特徴とする厚み状半導体装置。

【図3例6】 図3例1ないし2において、半導体素子は半導体素子の電極部の面をインターリードの第2面

に絶縁層を介してより固定されており、該半導体素子の電極部はワイヤにてインターリードの第1面と電気的に接続されていることを特徴とする厚み状半導体装置。

【図3例7】 図3例1ないし2において、半導体素子はパンプによりインターリードの第2面に固定されて電気的にインターリードと接続していることを特徴とする厚み状半導体装置。

## 【図4の概略図】

(0001)

【図4上の外周部材】 本図例は、半導体装置の断面に於いて、且つ、アフターリードの位置（スニュー）やアフターリードの厚み（コブラリテナー）の位置に於いて、リードフレームを用いた厚み状半導体装置に於ける。

(0002)

【図4の概略】 図4より用いられている厚み状半導体装置（プラスチックリードフレームパッケージ）は、一面に図15（a）に示されるような構造であり、

半導体素子1510を固定するダイパッド部1511の両側の面と電気的に接続を行うためのアフターリード部1513、アフターリード部1513に一体となったインターリード部1512、該インターリード部1512の先端部と半導体素子1520の電極部1521とを電気的に接続するためのワイヤ1530、半導体素子1520を固定して基板からの応力、熱膨張から保護する1540部からなっており、半導体素子1520をリードフレームのダイパッド1511の面に固定した状態で、基板1540により固定してパッケージとしたもので、半導体素子1520の電極部1521に於いて

図15（b）に示すような構造のもので、半導体素子を固定するためのダイパッド1511と、ダイパッド1511の両面に設けられた半導体素子とを固定するためのインターリード1512、該インターリード1512に固定して外周部材との電気的接続を行うためのアフターリード1513、厚み状半導体装置のダムとなるダム部1514、リードフレーム1510全体を支持するフレーム（部）部1515を備えており、且つ、コパール、42合金（42%ニッケル-6合金）、銅合金のような高強度に優れた金属材料を用い、プレス加工もしくはエッチング法により形成されている。図15（b）（c）は、図15（b）（d）に示すリードフレーム半導体装置のF1-F2における断面図である。

(0003) このようなリードフレームを用いた厚み状半導体装置（プラスチックリードフレームパッケージ）において、導子柱の先端部小径の形状と半導体素子の電極部小径の形状とを、小型化かつ電極部との

図15（b）（c）に示すような構造のもので、半導体素子を固定するためのダイパッド1511と、ダイパッド1511の両面に設けられた半導体素子とを固定するためのインターリード1512、該インターリード1512に固定して外周部材との電気的接続を行うためのアフターリード1513、厚み状半導体装置のダムとなるダム部1514、リードフレーム1510全体を支持するフレーム（部）部1515を備えており、且つ、コパール、42合金（42%ニッケル-6合金）、銅合金のような高強度に優れた金属材料を用い、プレス加工もしくはエッチング法により形成されている。図15（b）（c）は、図15（b）（d）に示すリードフレーム半導体装置のF1-F2における断面図である。

(0004) このようなリードフレームを用いた厚み状半導体装置（プラスチックリードフレームパッケージ）において、導子柱の先端部小径の形状と半導体素子の電極部小径の形状とを、小型化かつ電極部との







で、テーピングの工程や、リードフレームを固定するクランプ工程で、ベタはに腐蝕され部分的に腐った部分との腐蝕が顕著になる場合があるので、エッチングを行うエリアはインターリード穴の追加加工部分だけにせず大めにとらねばならない。従って、温度57°C、濃度8 g/lの塩化第二硫酸を用いて、スプレーで2.5 kS/cm<sup>2</sup>にて、レジストパターンが形成されたリードフレームを1110の濃度をエッチングし、ベタは(平電板)に固定された第一の凹部1150の腐蝕がリードフレーム厚の約2/3程度に達した時点でエッチングを止めた。(図11(d))

上述第1回目のエッチングにおいては、リードフレーム厚1110の表面から同時にエッチングを行ったが、必ずしも同時にエッチングする必要はない。本実施例のように、第1回目のエッチングにおいてリードフレーム厚1110の表面から同時にエッチングする理由は、表面からエッチングすることにより、後述する第2回目のエッチング時間を短縮するため、レジストパターン9202域からのみの表面エッチングの場合と比べ、第1回目エッチングと第2回目エッチングのトータル時間が短縮される。従って、第一の凹部1130の凹部に固定された第一の凹部1500にエッチング液を1180としてのエッチング液のあるホットメルトコックス(ブレンデッド元素と塩化コックス、22MR-WB6)を、ダイコートを流して、塗布し、ベタは(平電板)に固定された第一の凹部1150に埋め込んだ。レジストパターン1120A上にもエッチング液を1180に塗布された状態とした。(図11(c))

エッチング液を1180を、レジストパターン1120A上全面に塗布するのではなく、第一の凹部1150を含む一面にのみ塗布することにした。図11(c)に示すように、第一の凹部1150とともに、第一の凹部1130凹部にエッチング液を1180を塗布した。本実施例で採用したエッチング液は、1180は、アルカリ性塩基のワックスであるが、基本的にエッチング液に粘性があり、エッチング時に腐蝕の

腐蝕性のあるものが、好ましく、特に、上述ワックスに固定された、U.V.硬化型のものが好ましい。このようにエッチング液を1180をインターリード穴の凹部を形成するためのパターンが形成された凹部の凹部を第一の凹部1150に塗布することにより、後述までのエッチング時に第一の凹部1150が腐蝕されて太くならないようにしていることと、表面からエッチング加工に対して腐蝕的な腐蝕性を示すため、スプレーを流す(2.5 kS/cm<sup>2</sup>以上)とすることができ、このことによりエッチングが容易に進行したくなる。この後、第2回目のエッチングを行う。ベタは(平電板)に固定された第二の凹部1160を凹部からリードフレーム厚1110をエッチングし、上述で、

インターリード穴を1131Aを形成した。(図11(c))

第1回目のエッチング加工にて形成された、リードフレーム面に形成したエッチング液面は腐蝕であるが、この面を第2回はインターリード部にへこんだ凹部である。従って、通常、エッチング液を9202のレジスト厚(レジストパターン1120A、1120B)の厚さを示し、インターリード穴を1131Aが形成された図9(a)に示すリードフレーム1130Aを410、エッチング液を1180とレジスト厚(レジストパターン1120A、1120B)の厚さを示したトリクル処理により腐蝕した。

(0014) 上述、図11に示すリードフレームの腐蝕状態に、本実施例に用いられる、インターリード穴を同時に形成したリードフレームをエッチング加工により腐蝕する方式で、特に、図1に示す、インターリード穴の第1凹部1131Aを同時に腐蝕する方式と同一面に、第2凹部1131Aと対向させて形成し、且つ、第3凹部1131Aと、第4凹部1131Aをインターリードの内部に向かって凹んだ凹部にエッチング加工方式である。従って、本実施例の方式は従来のようにパンプを流して腐蝕液をインターリードの第2凹部1131Aに形成し、インターリードと電気的に接続する場合に

に、第2凹部1131Aをインターリード部に凹んだ凹部に形成した方がパンプ腐蝕の腐蝕の腐蝕が太くなる。図12に示すエッチング加工方式が図られる。図12に示すエッチング加工方式は、第1回目のエッチング工程までは、図11に示す方式と同じであるが、エッチング液を1180を第二の凹部1160の凹部に埋め込んだ後、第一の凹部1150から第2回目のエッチングを行い、腐蝕を促進している。従って、第1回目のエッチングにて、第二凹部1140からのエッチングを充分に促して、図12に示すエッチング加工方式によって得られたリードフレームのインターリード部の腐蝕状態は、図6(b)に示すように、第2凹部1131Aがインターリード部にへこんだ凹部になる。

(0015) 図11、図12に示すエッチング加工方式のように、エッチングを2段階にわたって行うエッチング加工方式を、一面には2段階エッチング加工方式とっており、本実施例に有利な加工方式である。本実施例に用いた図9(a)に示す、リードフレーム1130Aの腐蝕においては、2段階エッチング加工方式で、パンプを流すことにより部分的にリードフレーム厚を腐蝕しながら腐蝕を促進する方法とが併用して行われており、リードフレーム厚を腐蝕した部分においては、特に、腐蝕加工が促進するようにして、図11、図12に示す、上述の方式においては、インターリード穴を1131Aの形成加工は、第二の凹部1160の凹部と、電気的に接続されるインターリード穴の腐蝕に有利な腐蝕である。例えば、図11に示す50μm

の両方に平等ではあるが、この部分の両方ともは  
 ペスとくれない。また両方ともリフトプレーンに  
 である、両方（ボンディング）両方に平等なミ  
 チングを平等とみる。図13（二）にプレス（ニ  
 ー）によりインナーリードを両方に同時に  
 チングが二によりインナーリードを同時に  
 1331Dを加えたものの、二を同時に（図13  
 との両方（ボンディング）を示したものであるが、こ  
 れはプレスが同時に示すように平等になってい  
 た。どちらの両方を用いて両方（ボンディング）し  
 6、図13（二）の（a）、（b）に示すように両  
 （ボンディング）の両方に両方がよく品質の両方  
 なる両方が多い。図1331Dは二に両方

10 たので、どちらの面を用いて成形（ボンディング）して  
も、図11（二）の（a）、（b）に示すように成形  
（ボンディング）の際に成形面が歪く品質的にも問題  
なう場合が多い。故、1321.A.Bはニエニング面であ  
る。

（0018）次に成形面1の成形防止型ニエニング面の成形  
面を挙げ、図1（a）～図3（c）に、その成形  
に成形面1の成形防止型ニエニング面の成形面を  
用いる。図1（a）に示す成形面1のニエニング面は、成形面  
1のニエニング面とは、タイプ1のニエニング面とは異な

もで、ダイパッド図1305が外空に存在している。ダイ  
パッド図1305が外空に存在していることにより、天  
板例1)に比べ、他の見知性が保たれている。図3(b)  
に示す変形例の構造は基本型、ダイパッド図1305が外空  
に存在させているものであり、天板例1)に比べ、他の見  
知性が保たれている。変形例1や図3(a)に示す変形例  
とは、基本型より110の向きが異なり、ワイヤボンデ  
イング面をリードフレームの裏面に付けている。図3  
(c)、(d)、図3(e)、図3(f)に示す変形例は、それぞれ  
変形例1、図3(a)に示す変形例、図3(b)  
に示す変形例において、基本型の電からなる導子部を反  
転し、導子部の面を基板層下部として用いているもので  
あり、前述二例を応用した構造となっている。  
[0019] 次いで、変形例2の導子部防止型と基本型と  
を比較する。図4(a)に変形例2の導子部防止型と基本型  
との断面図があり、図4(b)に図4(a)のA-A'  
におけるインターリード部の断面図で、図4(c)は  
図4(a)のB-B'における導子部部の断面図であ  
る。尚、変形例2の導子部防止の外観は変形例1とほぼ  
同じとなるため、図には省略した。図4中、270の位置は導  
子部、210は導子基座、211は導子部（パッ  
ド）、220はワイヤ、230はリードフレーム、231  
はインターリード、232はA-A'に於いて、233はB-B'  
に於ける、234はC-C'に於ける、235はD-D'に於ける、  
236は導子部、237はA-A'に於ける、238はB-B'  
に於ける、239はC-C'に於ける、240はD-D'に於ける  
面、2335は上表面、240は下表面、270は  
導子部防止テープあり、変形例2の導子部防止におい  
ては、リードフレーム230にダイパッドを用いたのでは  
なく、導子基座210にインターリード233とこれに  
対応する導子部270により固定されてあり、基本  
型より210は、導子部防止の断面図(パターン)211



10023) であり、表第4の第18列型と等価な面を  
 表わす。図7 (a) は表第4の第18列型と等価な  
 面の断面図であり、図7 (b) は図7 (a) のA7-A  
 8におけるインターリード面の断面図で、図6 (c) は  
 図6 (a) の87-98に於ける底平面的断面図であ  
 る。但し、表第4の第18列型の図中表第11とは  
 一致となる。図6を比較した、図7中、400は主面  
 面、410は副面面、411はパッド、430は



190  
 260  
 270  
 350  
 470  
 1110  
 1120A, 1120B  
 1130  
 1140  
 1150  
 1160  
 1170  
 1180  
 1320B, 1320C, 1320D  
 1321B, 1321C, 1321D  
 1331B, 1331C, 1331D  
 1331A

1331A  
 1410  
 1420  
 1430  
 1440  
 1510  
 1511  
 1512  
 1512A  
 1513  
 1514  
 1515  
 1520  
 1521  
 1530  
 1540

ードフレーム面

1331A

イニング面

1410

ードフレーム面

1420

オトレジスト

1430

ジストパターン

1440

ンターリード

1510

ードフレーム

1511

イパッド

1512

ンターリード

1512A

ンターリード先封

1513

クターリード

1514

ムバー

1515

レーン面 (内部)

1520

1521

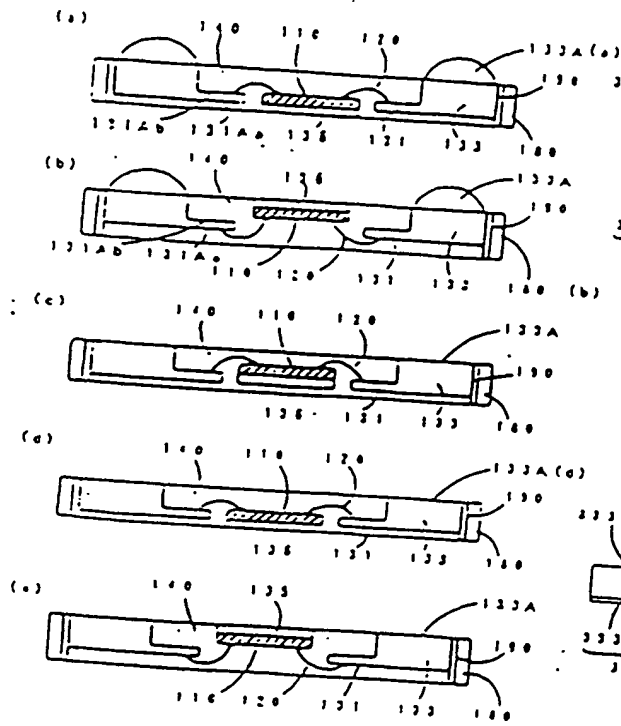
1530

1540

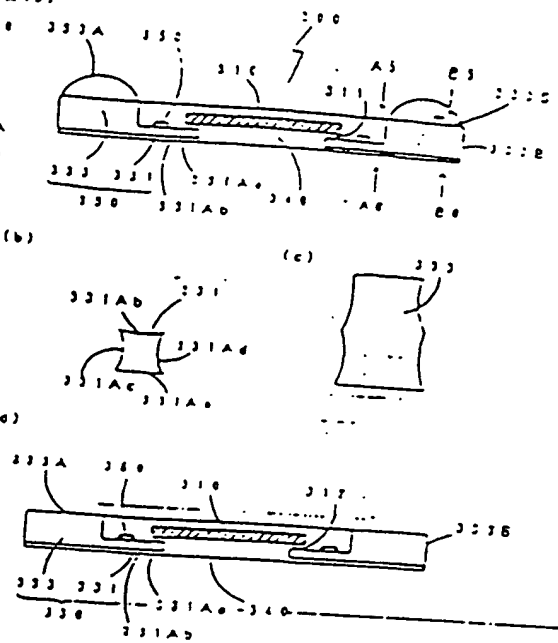
止角面



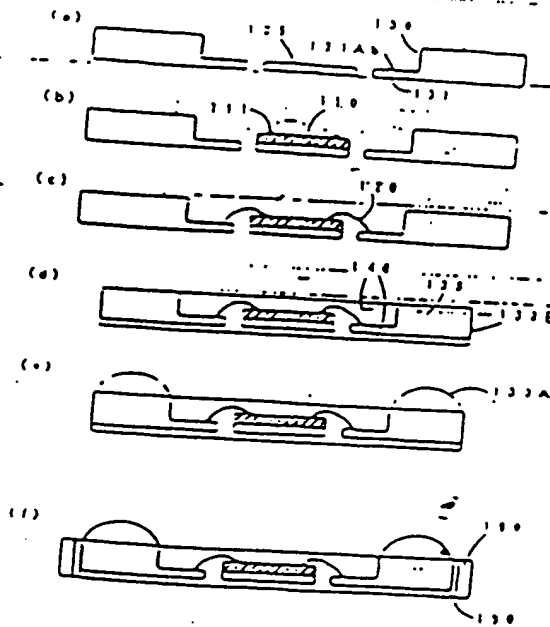
(22)



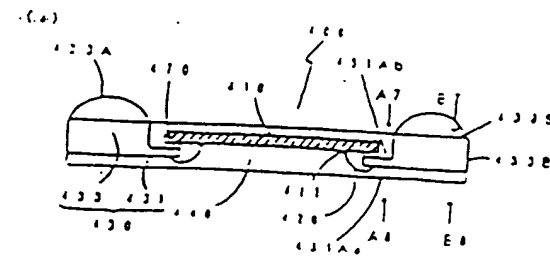
(26)



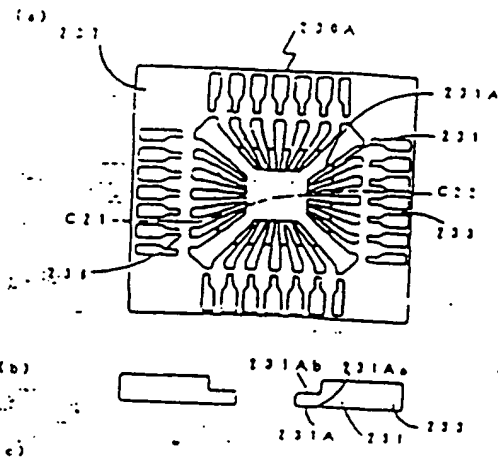
(23)



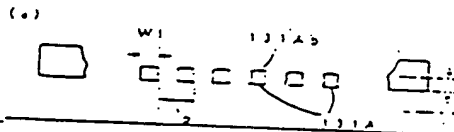
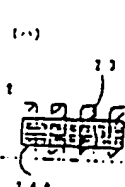
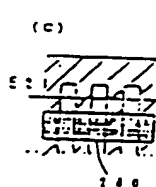
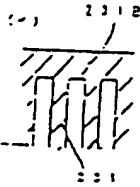
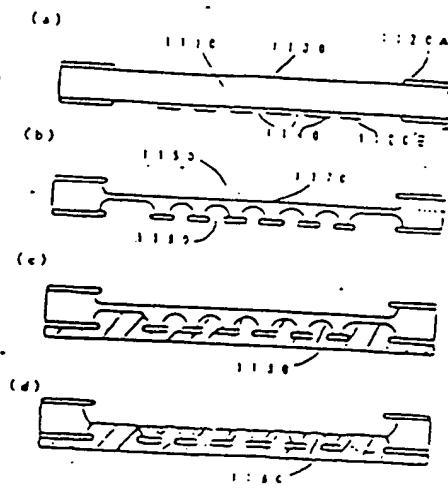
( ३१ )



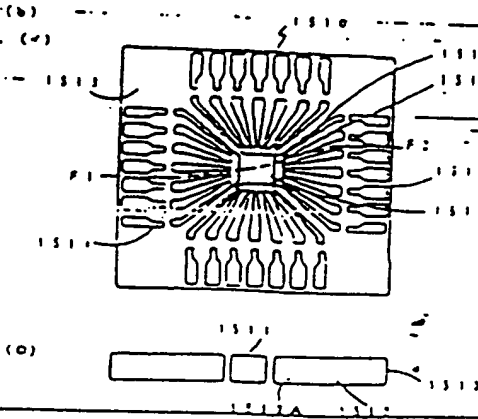
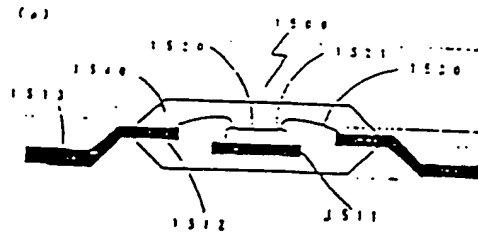
(210)



(212)



(215)



(21)

